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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,179	06/30/2003	Kerry Bernstein	BUR920010207US1	1178
23389	7590	09/22/2004	EXAMINER	
SCULLY SCOTT MURPHY & PRESSER, PC			LIN, SUN J	
400 GARDEN CITY PLAZA			ART UNIT	
GARDEN CITY, NY 11530			PAPER NUMBER	
			2825	

DATE MAILED: 09/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/604,179

Applicant(s)

BERNSTEIN ET AL.

Examiner

Sun J Lin

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 June 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 10-18 is/are rejected.
- 7) ☒ Claim(s) 7-9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06/30/2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input checked="" type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>6/30/03, 7/17/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is in response to application 10/604,179 filed on 06/30/2003.
Claims 1 – 18 remain pending in the application.

Specification Objections

2. The specification is objected to because of following informalities:
Paragraph 0007, line 6, change "rofitability" to **—profitability—**.
Paragraph 0015, line 3, change "the circuits" to **—circuits included in the integrated circuit—**.
Paragraph 0015, line 5, change "andthose" to **—and those—**.
Paragraph 0025, line 4, change "product"s" to **—product's—**.

Appropriate correction is required.

Drawing Objections

3. Drawings are objected to because of following informalities:
Fig. 1 – 5 are objected to due to reasons listed in *Notice of Draftsperson's Patent Drawing Review (PTO-948)* attached with this *Detailed Action*.
Fig. 1 should be labeled as a **—(PRIOR ART)—**.
Fig. 2 should be labeled as a **—(PRIOR ART)—**.
Fig. 3 should be labeled as a **—(PRIOR ART)—**.

Appropriate correction is required.

Claim Objections

4. Claims listed below are objected to because of the following informalities:
Claim 1, line 3, change "the circuits" to **—circuits included in the integrated circuit—**.
Claim 2, line 1, change "A method" to **—The method—**.
Claim 3, line 1, change "A method" to **—The method—**.
Claim 4, line 1, change "A method" to **—The method—**.

- Claim 5, line 1, change "A method" to **—The method—**.
Claim 6, line 1, change "A method" to **—The method—**.
Claim 7, line 1, change "A method" to **—The method—**.
Claim 8, line 1, change "A method" to **—The method—**.
Claim 9, line 1, change "A method" to **—The method—**.
Claim 10, line 2, change "the circuits" to **—circuits included in the integrated circuit—**.
Claim 11, line 1, change "A system" to **—The system—**.
Claim 12, line 1, change "A system" to **—The system—**.
Claim 13, line 1, change "A system" to **—The system—**.
Claim 14, line 4, change "the circuits" to **—circuits included in the integrated circuit—**.
Claim 15, line 1, change "A program" to **—The program—**.
Claim 16, line 1, change "A program" to **—The program—**.
Claim 17, line 1, change "A program" to **—The program—**.
Claim 18, line 1, change "A program" to **—The program—**.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(a) that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1, 3 – 6, 10, 12 – 14 and 16 – 18 are rejected under 35 U.S.C. 102(a) as being unpatentable over IEEE paper entitled "A Systemic Approach to SER estimation and Solutions" to Nguyen et al.

7. As to Claim 1, Nguyen et al. teach the following subject matter:

- A system approach to SER (soft error rate) estimation and solutions to latches/flip-flops and combinational logic (circuits) in a chip (i.e., integrated

circuit) – [abstract, page 60, left column, 1st paragraph]; Soft errors origin and simulation – [page 60, right column, bottom paragraph]; Notice that the soft error simulation is a method of simulating the integrated circuit (chip) on its SER performance, and the **SER estimation is a soft error analysis of (latches/flip-flops and combinational logic) circuits in the integrated circuit (chip)**;

- SER estimation (i.e., soft error analysis) should include a wide range of considerations, from the circuit responses to an injected charges up to architectural behavior – [page 60, right column, 2nd paragraph];
- A **measured SER is FIT (failure in time) rate** – [page 60, left column, 2nd paragraph]; timing derating is one of three components which make up of estimated FIT rate of a circuit element – [page 60, right column, 3rd, 5th paragraph]; different circuits (latched etc.) need different timing derating considerations (i.e., timing criteria) – [page 64, right column, 1st paragraph]; Timing derating factors are often derived from equations... based on the setup and hold (timing) windows of latched/flip-flops and the clock period – [page 69, left column, 4th paragraph]; Path analysis and timing data – [page 68, left column, 6th paragraph]; Notice that **timing derating factor is obtained through performing timing analysis and the timing derating considerations are timing criteria**;
- FIT rate of circuits are estimated based on **critical charge Q_{crit}** values using circuit simulation ... The minimal injected charged that causes (latch) failure is defined as Q_{crit} , the **critical charge that causes latch (circuit) failure** – [page 62, right column, "Nominal FIT Estimation"]; Notice that the as Q_{crit} value may not the same for different for different circuits; Therefore, the **SER estimation (soft error analysis)** of the circuits is performed to determine whether they meet specified **soft error criteria** (i.e., **having charge less than critical charge Q_{crit}**);
- SER solutions, SER-resistant latch (circuit) designs – [page 69, right column, 2nd, 4th paragraph]; Notice that the SER solutions is utilized to improve the circuits that fail the soft error analysis in order to achieve **SER-resistant** (i.e., **resistance to soft errors**) circuits.

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

8. As to Claim 10, reasons are included in **[Response A]** given above. Notice that the explanations included in **[Response A]** can be utilized in forming a system having means for simulating an integrated circuit as recited in Claim 10.

9. As to Claim 14, reasons are included in **[Response A]** given above. Notice that the explanations included in **[Response A]** can be utilized in generating a program of instructions readable and executable by machine to perform method steps for simulating an integrated circuit as recited in Claim 14.

10. As to Claims 3 and 12, as explained in **[Response A]**, *Nguyen et al.* teach the following subject matter:

- timing derating factor is obtained through performing timing analysis – **[Response A]**;
- timing derating factor is one of three components that make up of estimated FIT(failure in time) rate of a circuit – [page 60, right column, 3rd paragraph]; Therefore, FIT rate is estimated after the step of performing a timing analysis;
- FIT rate is soft error rate (SER) – **[Response A]**; therefore, soft error analysis is done after the step of performing a timing analysis.

11. As to Claims 4, 13 and 16, *Nguyen et al.* teach that FIT estimation and timing derating (i.e., timing analysis) could be done at late stage of design – [page 68, left column, 3rd, 6th paragraph]. Therefore, a further timing analysis of the improved circuits is performed to determine whether the improved circuits still meet the specified timing criteria.

12. As to Claims 5 and 17, as explained in **[Response A]**, the purpose of performing FIT estimation is to determine SER (soft error rate). Therefore, after the step of performing a further timing analysis, a further soft error analysis of the improved circuits

is performed to determine whether the improved circuit now meet the soft error criteria similar to that explained in [Response A].

13. As to Claims 6 and 18, Nguyen et al. teach identifying high FIT contributors (i.e., circuits having high SER) that can be fixed by small effort – [page 68, right column, 3rd Paragraph]. It means that those circuits that fail the further soft error analysis are further improved to further improve their resistance to soft errors similar to that as explained in [Response A].

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- (1). Determining the scope and contents of the prior art.
- (2). Ascertaining the differences between the prior art and the claims at issue.
- (3). Resolving the level of ordinary skill in the pertinent art.
- (4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

15. Claims 2, 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over IEEE paper entitled “A Systemic Approach to SER estimation and Solutions” to Nguyen et al. in view of IEEE paper entitled “Analyzing soft errors in leakage optimized SRAM design” to Degalahal et al.

16. As to Claim 2, Nguyen et al. teach all subject matter recited in Claim 1, Nguyen et al. also teach nominal FIT rate (i.e., SER) of a circuit depends on node capacitance and VDD value (i.e., power supply) of circuits – [page 60, right column, 4th paragraph]. Nguyen et al. do not teach a method of improving the circuits that fail the soft error

analysis by either having an additional voltage source or altering the capacitance of the circuits. Degalahal et al. discloses a method to estimate the SER (soft error rate) in CMOS SRAM circuits in [Eq. 1].

Degalahal et al. also teach the following subject matter:

- SER is inversely proportional to critical charge Q_{crit} – [Eq. 1];
- Q_{crit} is proportional to node capacitance and supply voltage (i.e., voltage source) – [page 228, right column, 4th paragraph];
- Q_{crit} at a node will decrease as supply voltage (voltage source) or node capacitance reduces – [page 228, right column, 4th paragraph];
- The nodal capacitance is strongly dependent on the layout – [page 228, right column, 4th paragraph – page 229, left column, 1st paragraph]; Notice that the nodal capacitance can be increased by altering the layout at the node.

Notice that, the additional supply voltage and larger nodal capacitance can be used to increase the threshold value of critical charge Q_{crit} thereby minimizing the SER performance.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teachings of Degalahal et al. either in including an additional voltage source or altering nodal layout to increase nodal capacitance in order to increase the threshold value of critical charge Q_{crit} thereby minimizing the SER performance to improve the circuits that fail the soft error analysis.

For reference purposes, the explanations given above in response to Claim 2 are called **[Response B]** hereinafter.

17. As to Claims 11 and 15, reasons are included in **[Response B]** given above.

Allowable Subject Matter

18. Claim 7 – 9 are objected to as being dependent upon a rejected base claim, but they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because the prior art does not teach or fairly suggest the following subject matter:

- The method according to Claim 6, wherein the further improving step included the step of further improving those circuit that fail the further soft error analysis using one of two defined procedures depending on whether the circuits pass or fail the further timing analysis in combination with other limitations as recited in Claim 7;
- The method according to Claim 6, wherein: a first set of circuits fail the further timing analysis and fail the further soft error analysis, a second set of circuits pass the further timing analysis and fail the further soft error analysis in combination with other limitations as recited in Claim 9.

Conclusion

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sun J. Lin whose telephone number is (571) 272-1899. The examiner can normally be reached on Monday-Friday (9:00AM-6:00PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Sun James Lin
Art Unit 2825
September 14, 2004

